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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,381	07/14/2003	Rajendra D. Pendse	CPAC 1015-1	5430

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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,381	PENDSE, RAJENDRA D.	
	Examiner	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *24-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/2/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I (Claims 1-23) in the reply filed on September 9, 2004 is acknowledged.

Drawings

2. Figures 1-2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are, not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, 10, 14, 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Shenoy (U.S. Patent No. 6,310,386). With regard to Claim 1, Shenoy discloses a chip-scale integrated

circuit chip package (column 5, lines 55-57) comprising a die (310) mounted by flip-chip interconnection (column 8, line 49) to a package substrate (307), the package substrate being a laminate (column 8, lines 50-53) comprising a dielectric layer (304) having a single conductive trace layer (305) on a first surface thereof (figure 3A) and an active ground plane (302) overlying a second surface thereof (figure 3A), wherein the ground plane is electrically connected to ground sites at the first surface of the dielectric layer through openings (308) in the dielectric layer (column 9, lines 2-6 and figure 3A), and wherein second level interconnects are on the first surface of the dielectric layer (column 8, line 67 and column 9, lines 1-2), and the die is mounted on the first surface of the dielectric layer (figure 3A).

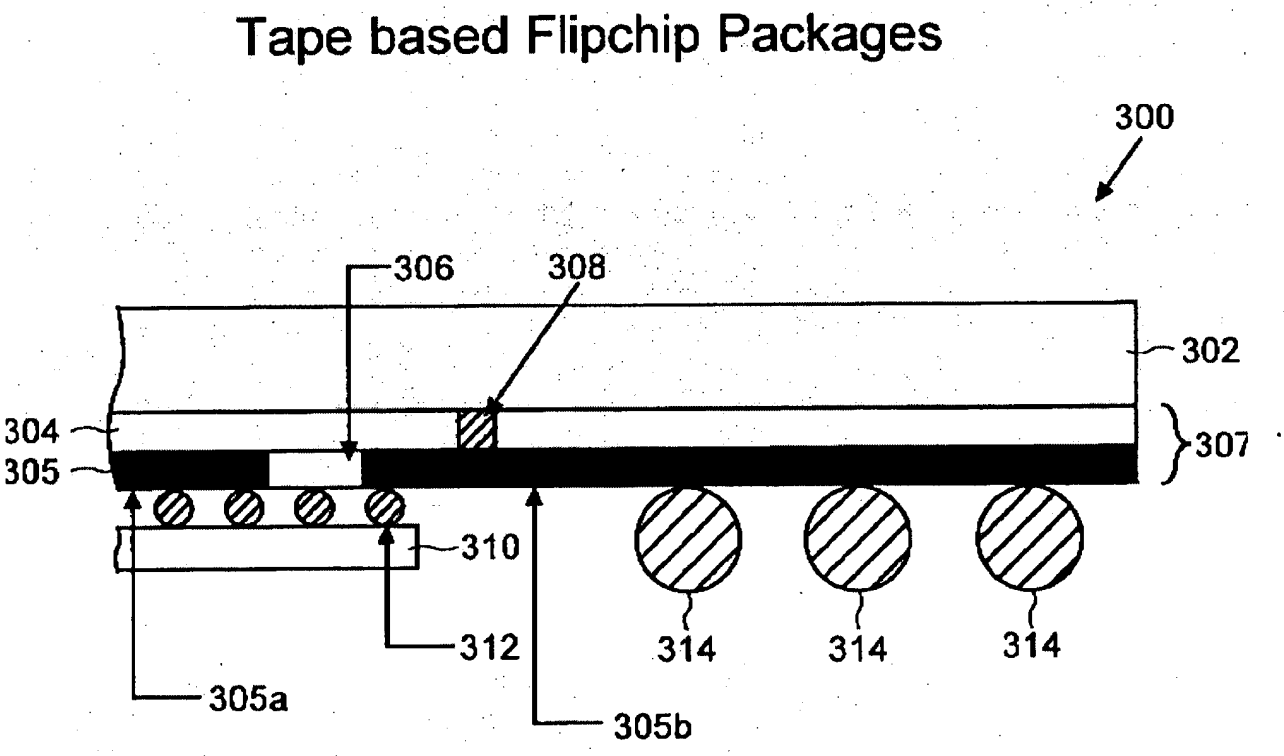

FIG. 3A

With regard to Claim 2, Shenoy discloses openings (308) in the dielectric layer (304) that are filled with an electrically conductive material (column 9, lines 2-6).

With regard to Claim 7, Shenoy discloses a ground plane (302) that comprises an electrically conductive film overlying the second surface of the dielectric layer (column 8, line 50; column 9, lines 5-6 and figure 3A).

With regard to Claim 10, Shenoy discloses a ground plane (302) that is disposed directly upon the surface of the dielectric layer (304) on the dielectric side (column 8, lines 50-53 and figure 3A).

With regard to Claim 14, Shenoy discloses a ground plane (302) that comprises a metal (column 9, lines 2-6).

With regard to Claim 20, Shenoy discloses a die (310) that is provided with interconnection bumps (312) affixed to an arrangement of connection sites in a first surface of the die (column 8, lines 65-67) and a conductive trace layer (305) that is provided with a complementary arrangement of interconnect sites (column 8, lines 51-62), and a flip-chip interconnection (column 8, lines 43-44 and 49-50) in a solid state interconnection.

With regard to Claim 21, Shenoy discloses a die (310) that is attached (column 8, lines 65-67) at about a center of the first side (figure 3A) of the substrate (307), and solder balls (314) for

second level interconnections that are located nearer the periphery of the first side of the substrate.

With regard to Claim 22, Shenoy discloses electrical traces that are formed within an interconnect layer (305) in the first surface of the package substrate (307), and the traces fan outward from the interconnect pads to the solder ball (314) attachment sites, (column 8, lines 52-56 and figure 3A).

With regard to Claim 23, Shenoy discloses some of the traces constructed as coplanar waveguides (column 8, lines 44-48), each comprising ground lines alongside a signal line (column 8, lines 60-62) on a coplanar dielectric material (figure 3A).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy (U.S. Patent No. 6,310,386) in view of Pasch (U.S Patent No. 5,468,681). With regard to Claims 3-6, Shenoy essentially discloses the claimed invention but fails to show, the claimed electrically conductive materials filling the openings.

However, Pasch discloses a semiconductor manufacturing technique employed in flip-chip devices (column 1, lines 29-32) which includes through-holes filled with conductive material, such as metal, solder, or conductive polymer or epoxy, such as silver-filled epoxy (column 11, lines 59-63).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed electrically conductive materials filling the openings, as suggested by Pasch, in order to provide an improved technique for packaging semiconductor dies and for interconnecting the packaged dies to external systems (column 11, lines 30-32).

With regard to Claims 8-9, a further difference between the claimed invention and Shenoy is, the ground plane and the electrically conductive fill material being made from either the same or different materials. However, Pasch discloses a semiconductor manufacturing technique employed in flip-chip devices (column 1, lines 29-32) which includes through-holes filled with conductive material, such as metal, solder, or conductive polymer or epoxy, such as silver-filled epoxy (column 11, lines 59-63).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed ground plane and the electrically conductive fill material being made from either the same or different materials, as suggested by Pasch, in order to provide a ground plane made of

metal and openings filled with metal, or in the alternative, a ground plane made of metal and openings filled with solder, or conductive polymer or epoxy, such as silver-filled epoxy, as needed for the semiconductor package characteristics.

Claims 11, 15 and 17 rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy (U.S. Patent No. 6,310,386) in view of Laine et al. (U.S. Patent No. 5,939,783). With regard to Claim 11, Shenoy essentially discloses the claimed invention but fails to show, the claimed ground plane being disposed upon a conductive film formed over the dielectric side of the dielectric layer.

However, Laine discloses an electronic package (10) including a ground plane (11), (column 4, lines 56-58), that is disposed upon a conductive film (17) over a dielectric layer (19), (figure 1).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed ground plane being disposed upon a conductive film formed over the dielectric side of the dielectric layer, as suggested by Laine, in order to provide a device with high-density circuitry while also assuring thermal-match (column 10, lines 39-44).

With regard to Claims 15 and 17, a further difference between the claimed invention and Shenoy is, the claimed ground plane comprising aluminum or copper.

However, Laine discloses an electronic package (10) including a ground plane (11), (column 4, lines 56-58), that comprises aluminum or copper (column 4, lines 20-21).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed ground plane comprising aluminum or copper, as suggested by Laine, in order to provide a ground plane comprising a thermally conductive and substantially planar member (column 4, lines 19-20).

Claims 12-13 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy (U.S. Patent No. 6,310,386) in view of Karnezos (U.S. Patent No. 6,373,131). With regard to Claim 12, Shenoy essentially discloses the claimed invention but fails to show, the claimed ground plane disposed upon an adhesive layer formed on the dielectric side of the dielectric layer.

However, Karnezos discloses a semiconductor package (column 7, lines 31-33) including a ground plane (160) that is disposed upon an adhesive layer (124) formed over the dielectric side of a dielectric layer (125), (figure 3A).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed ground plane disposed upon an adhesive layer formed on the dielectric side of the

dielectric layer, as suggested by Karnezos, in order to secure a dielectric layer to a ground plane (column 8, lines 5-7).

With regard to Claim 13, a further difference between the claimed invention and Shenoy is, an adhesive layer comprising an electrically insulating adhesive layer.

However, Karnezos discloses an adhesive layer (124) that is a pressure-sensitive adhesive (column 10, lines 58-60).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed adhesive layer comprising an electrically insulating adhesive layer, as suggested by Karnezos, in order to secure a dielectric layer to a ground plane (column 8, lines 5-7).

With regard to Claim 18, a further difference between the claimed invention and Shenoy is, the claimed gap between a die and a substrate that is at least partially filled with a die-attach material.

However, Karnezos discloses a gap (figure 3A) between a die (112) and a substrate (150) that is at least partly filled with a die-attach material (113), (column 7, lines 54-57).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed gap between a die and a substrate that is at least partially filled with a die-attach material, as suggested by Karnezos, in order to provide a die-attach adhesive with excellent thermal and electrical conductivity (column 7, lines 57-61).

With regard to Claim 19, a further difference between the claimed invention and Shenoy is, the claimed die-attach material comprising an epoxy.

However, Karnezos discloses a die-attach material (113) comprising an epoxy (column 7, lines 57-59).

Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed die-attach material comprising an epoxy, as suggested by Karnezos, in order to provide a die-attach adhesive with excellent thermal and electrical conductivity (column 7, lines 57-61).

Claim16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shenoy (U.S. Patent No. 6,310,386) in view of Kinsman (U.S. Patent No. 6,002,165). With regard to Claim 16, Shenoy essentially discloses the claimed invention but fails to show, the claimed ground plane comprising nickel.

However, Kinsman discloses a semiconductor package (column 2, lines 10-12) including a ring plate (46) serving as a ground plate (column 2, lines 35-38) and comprising nickel (column 4, lines 13-15).

Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as disclosed by Shenoy to include the claimed ground plane comprising nickel, as suggested by Kinsman, in order to provide a ground plate comprising a highly conductive material (column 4, lines 13-14).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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